

§73. Development of High Performance Control System by Decentralization on QUEST

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The computer for the plasma control acquires various types of data such as plasma current, magnetic signals, and visible light. This also calculates various control signals such as coil currents, RF power, and piezo valves, and controls them. These acquired and control signals are not independent from each other but have a relationship with each other. Thus, the plasma control system (WS) is desirable in nature to be a centralized controls system which acquires all kinds of data and control all subsystems. However, this sometimes becomes over loaded with the WS. In actual, the WS of QUEST acquires various data and controls various subsystems with calculating plasma equilibrium and processing the plasma image using 1.73 GHz Intel Core i7-820 quad core CPU. All of these tasks use almost full CPU resource, and make it impossible to impose another control term any more.

In order to resolve these technical issues, a distributed control system is developed, which is composed of several control system and enables the implementation of more versatile controls. Each control system is connected to each other via reflective memories with optical fiber cables. The advantage is to provide the electrical isolation spontaneously. With the centralized control system, all the input and output signals are transferred via the electrical isolation amplifier to avoid mixed reference potentials. However, in the distributed system, there is no need to prepare the expensive broadband isolation amplifiers.

Figure 1 shows the current status of the CPU usage with the centralized control system. A thread `L_AIO_1` enclosed with a dashed line in Fig. 1 denotes the data transfer with DMA FIFO between the control module and 4 FPGA (Field Programmable Gate Array) modules. Each

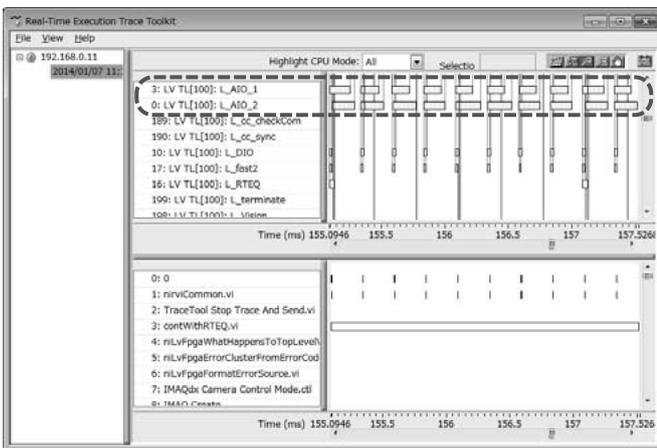


Fig. 1. Usage monitoring of control system's Quad Core CPU.

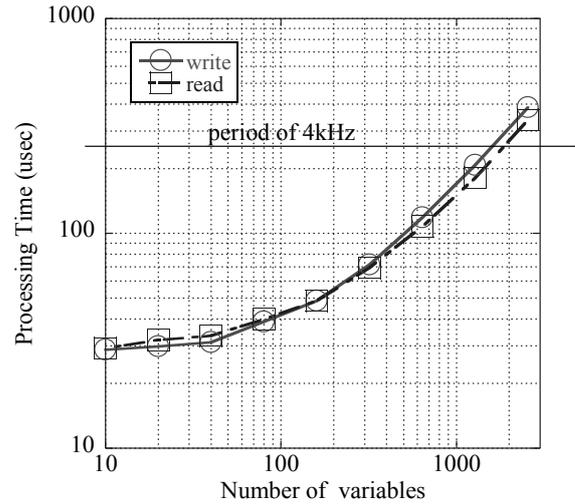


Fig. 2. Time to read and write a reflective memory

FPGA module has 8 analog and 8 input channels. A thread `L_AIO_2` is also the data transfer of 4 FPGA modules with 100 kHz numerical integration of magnetic signals. These threads are executed in 4 kHz (250 usec). The bars in Fig. 1 denote CPU occupation of 4 cores. The latter thread takes more time than the former because numerical integrated data have to be transferred in addition. (Notes: The numerical integration is executed on FPGA and does not put a load on CPU.) With these two threads, almost two cores are occupied, and the main thread, the equilibrium calculation thread, and the plasma image processing use other cores. Thus, almost full cores are used, and the additional other control terms cannot be imposed to the WS in the present status.

The GE cPCI-5565PIORC of National Instruments Corp. is used as the reflective memory, which has 256 Mbytes on board SDRAM and can transfer 170 Mbytes/sec according to manufacturer catalog. In many cases, the data type to share between systems may be 8 byte double precision real data. Figure 2 shows the time to read and write the reflective memory with double precision real data measured on the WS. There is no difference between read and write time, and the time have relationship of offset linear on the amount of data. Especially, data amount of 1000 to 2000 can be shared with 4 kHz which is the operating frequency of the WS, and is sufficient, though the 64 double precision real data which contain 32 magnetic signals and 32 its numeral integrated data is to share for the mean time. This transfer rate is about 50 Mbytes/sec less than 170 Mbytes/sec of catalog. This may depends on data size to share or the data types.

In future, the fundamental data such as shot number, control status, and time will be shared between systems. And, many variety control terms will be implemented with the increased available capacity by using reflective memory.