§42-1 Development of New Data Processing System for High Repetition Nd:YAG Thomson Scattering Measurement

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Objective of development of new data processing system The Nd:YAG Thomson scattering (YTS) system requires a high speed data processing, because the short laser pulse width ($\sim 10ns$) is required for improvement of S/N ratio[1]. Until now, a charge to digital AD convertor (CDC) was commonly used as the data acquisition system of the YTS measurement. But this convertor is not necessarily the optimum one for the YTS. Recently, a high speed AD converter of 12 bits resolution and 500MHz sample rate (ADS5463, Texas Instruments inc.) had been developed, then we are developing the high speed YAG Thomson scattering AD Convertor (HYADC) that can directly convert the scattered light signal to the digital data[2].

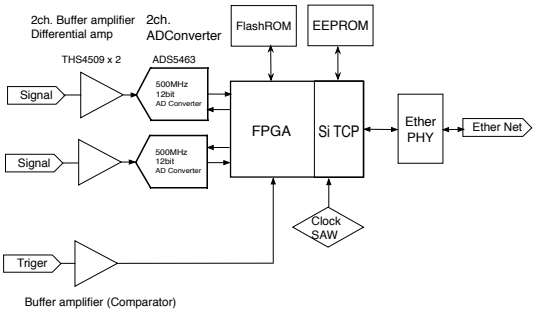

Fig. 1: Circuit diagram of The HYADC.

Data transfer of HYADC by SiTCP HYADC data transfer to the analysis system is executed by SiTCP, developed by KEK[3]. SiTCP can transfer the data recorded in the HYADC on the TCP/IP protocol performed by a logic circuit without CPU. The transfer rate of the SiTCP was verified as 95% of the theoretical maximum rate of the Ethernet, with the rate increased by future development of the Ethernet technique. Therefore, the transfer rate was sufficient to apply the YTS measurement to a real time feedback system for the plasma control[2].

As the SiTCP is based on a TCP/IP protocol, it is easy to construct a distributed data processing system of multichannel polychromators using switching hubs. Similarly, developing data transfer software using the socket procedure is easy, is supported by most computers, and can be controlled by EPICS[4], which is required in the ITER project. Because the SiTCP consists of a few chips, embedding it in the polychromators is easy.

Development of the HYADC The circuit diagram of the HYADC prototype is shown in Figure 1. The circuit has two analog to digital channels, which consist of two AD converter, two amplifiers, an FPGA and a physical layer chip for Ethernet communication. The almost all the logical circuits are integrated into the single FPGA. The present status of the development is as follows[2].

The design of the FPGA already has been completed: the structure of memory, register, acquisition from AD convertor and the data transfer system to a host computer are designed[2]. The HDL description of logical circuit, logical synthesis, and circuit layout for the FPGA has also been completed. An experimental prototype of the HYADC that is shown in Figure 2 is developed using evaluation boards for an initial test purpose. Test signal is successfully converted by a sampling frequency of 500MHz, and we confirm that the designed FPGA works correctly. Design of a substrate arrangement has been completed, then we are constructing the actual prototype of the HYADC. The prototype will be tested using the Nd:YAG Thomson scattering system of LHD and Heliotron J.

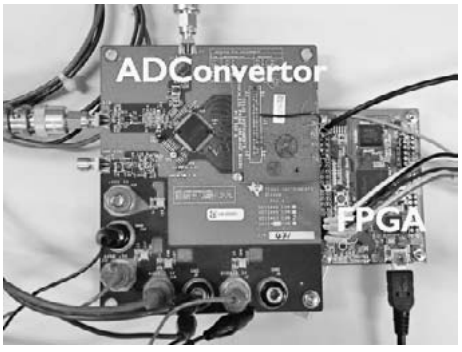

Fig. 2: Picture of the HYADC prototype using evaluation boards.

Acknowledgments
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1) T.Minami, S.Kobayashi, T.Mizuuchi, et al. 2010, Rev. Sci. Instrum., 81: 10D532

2) T.Minami, Y.Itoh, I.Yamada, et al. 2014, Rev. Sci. Instrum., 85: 11D837

3) U. Tomohisa, IEEE Transactions on Nuclear Science. vol. 55, no. 3, 2008.6, pp.1631-1637

4) EPICS can be referred in http://www.aps.anl.gov/epics/