§19. Development of Full Digital Processing Phase Detector for Interferometer

Minami, T. (Kyoto Univ.),
Nakanishi, H., Funaba, H., Yamada, I., Itoh, Y.,
Akiyama, T.

Objective of development of full digital processing phase detector for interferometer The interferometer for plasma line averaged density measurement is a basic diagnostic for the fusion plasma research. To solve the fringe jump problem is important for the interferometer, because the fault of the phase comparator is occurred in rapid density increase, for example, by the pellet injection. The objective of the development of new full digital processing phase detector is to solve the fringe jump problem by the new digital processing method. The new phase detector has the ability to measure the ultra-rapid phase change or the very small phase signal, which can not be measured by the previous one. The speed of the data conversion of the new phase detector is considerably faster than that of the previous one, and it also apply the density feedback control of the magnetic confined fusion plasma. The new phase detector can contribute to the fast density measurement of the LHD and Heliotron J experiments, and also to solve the physics of the fast plasma phenomena.

Design of full digital processing phase detector The previous analog phase detector converts the IF signal of the interferometer to the analog phase signal by a specific analog operational circuit. In contrast, the new full digital processing phase detector directly convert the IF signal to the digital signal by the fast A/D convertor, and the phase digital signal is calculated by a specific logical operational circuit. The previous analog phase detector utilizes the zero-cross timing signal to derive the phase difference signal. On the other hand, the full digital processing phase detector utilizes the I/Q convertor, and the phase difference signal is directly calculated form the IF signal itself. The fringe jump problem of the rapid density increase can be soluble in principle by utilizing the very fast pipe line A/D convertor of 500MHz.

Development of full digital processing phase detector The full digital processing phase detector is based on the fast 500MHz A/D convertor which is developed for the Nd YAG Thomson scattering measurement[1]. The logical operational circuit of the phase calculation is embedded in the control FPGA of the A/D convertor. In this fiscal year, we concentrate the development of a 500 MHz, 12 bits A/D convertor board, which consists of the A/D convertor, the control FPGA, SiTCP[2] of the data transfer. The design and the initial development of the first prototype of the A/D convertor board have been completed. Figure 1 shows the picture of the prototype A/D convertor board. The layout of the components on the substrate was carefully designed. The equal-length wiring reduces the delay-time between individual data transfer lines. The speed of the data processing is improved by the reduction of the parasitic capacitance of the wiring. The board has two A/D convertor channels, then the reference signal and the probe signal of the interferometer can be simultaneously processed. The board is controlled by the one FPGA chip (Spartan6 of Xilinx co.) which is mounted on the board center. The phase calculator will be embedded in the FPGA chip. Because the SiTCP circuit[2] is also mounted on the board, the data acquisition, the data processing and the data transfer can be simultaneously realized by only one small board. The future plan of the development is to check the basic operation of the board and to confirm the basic performance of the A/D conversion. We will concentrate to find bugs of the operation, and we will develop a next upgrade of the prototype board. The logical operational circuit of the phase calculation will be implemented in the FPGA chip. The initial test of the full digital processing phase detector will be carried out using the FIR interferometer of the Heliotron J.

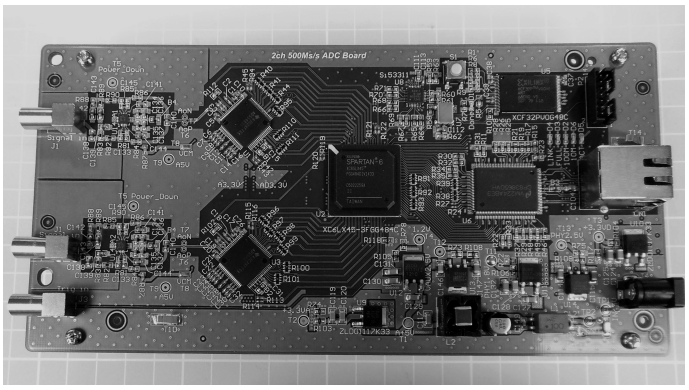

Fig. 1: Prototype of full digital processing phase detector board

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