# §21. Development of a Detector System for High-energy and Heavy Ions

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In LHD experiments, the heavy ion beam probe (HIBP) can be used to measure the electrostatic potential in the core region of LHD plasma. However, since the attenuation of the probe beam inside the plasma was severe under the present circumstances, the accurate measurement of the potential profiles in plasma with the electron density of 1.5 x $10^{19}$ $m^{-3}$ or higher was difficult. Moreover, in turbulence measurement, which requires high signal-to-noise ratio and temporal resolution, it only can be performed in quite low density plasma (~ 0.1 x $10^{19}$ $m^{-3}$). In order to study the plasma confinement of LHD, a higher precision measurement is required. In this study, we are developing the readout electronics of the front-end circuit with the specific integrated circuit (ASIC) in order to reduce electric noise and to construct multi-channel data readout system.

In the signal processing system requirements, the low noise and high gain amplifier and the low cross talk among channels were required. For the front-end circuits of high gain amplification which converted a small current (~$10^{-7}$ A) to the voltage, it is necessary to design the amplifiers closer to the detection device. Therefore, we decided to develop the readout electronics of the front-end circuit for the specific integrated circuit (ASIC). To develop the CMOS analog ASIC, the device parameters for the circuit simulator (SPICE) were done according to the ASIC manufacturing standard, and the circuits were redesigned. Based on the good result in SPICE, the design was proceed to the mask layout for the ASIC. In this fiscal year, the prototype of ASIC shown in Fig. 1. These circuits were using 700 nm rules process, supplied the voltage of 5V, and it was produced by NuvoTon Technology Corp. in Taiwan.

The evaluation test of the developed operational amplifier has been performed under the condition where the op-amp has been used as an amplifier with the gain of 10, and the linearity of the output and the frequency response have been evaluated. The configuration of the test bench is shown in Fig. 2. The results are summarized as follows; Gain: 19.7 dB, Offset voltage: +36 mV, Cut-off frequency: 1.2 MHz. Fig. 3 shows the output response when a sine wave at 100 kHz was input. It indicates good linearity. However, 0.002 % of the non-linearity appears as the output voltage exceeds approximately 4 V. From the point of view of signal-to-noise ratio and the resolution of digitizers, the increase in the maximum operating voltage and the function of the offset adjustment are desirable. In addition, the output response was distorted when the frequency of the input exceeds 400 kHz, though the frequency response of 500 kHz or more is required for the HIBP measurement. The ASIC is going to be redesigned for the higher frequency response and adjust the offset voltage in collaboration with the University of Tokyo VDEC (http://www.vdec.u-tokyo.ac.jp/)

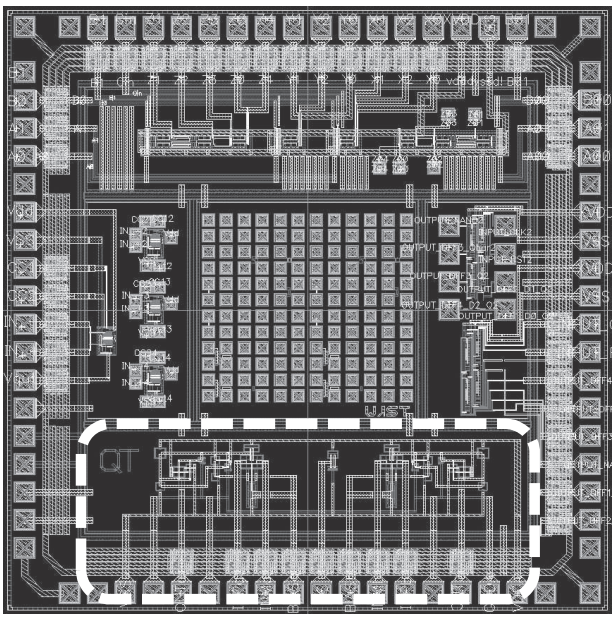

Fig. 1 A prototype of ASIC. The area enclsed by a white dashed curve consists of 2operational amplifiers.

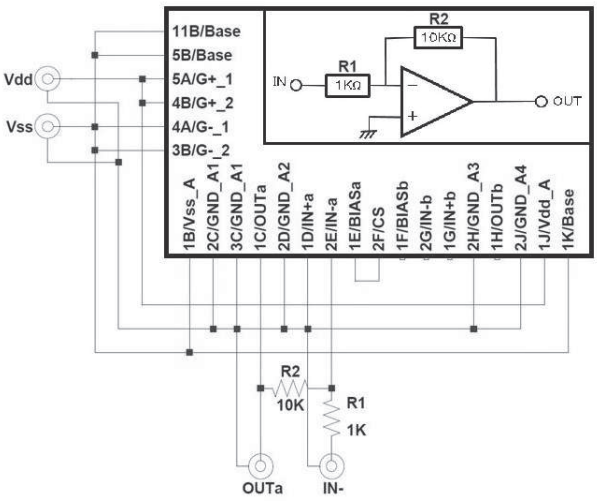


Fig. 2. Configuration of the test bench for evaluation test circuit of the prototype ASIC.

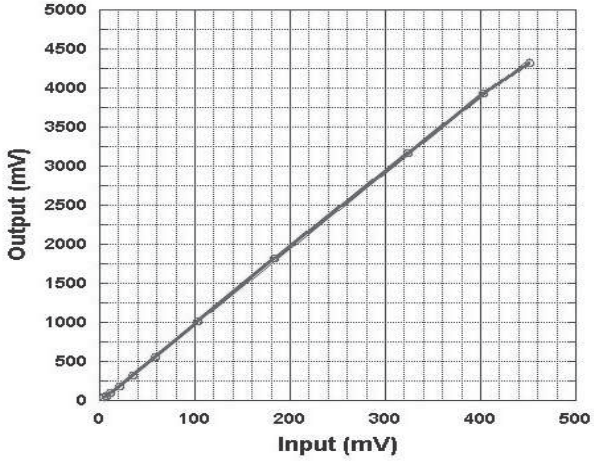


Fig. 3. Linearity of output response at the frequency of the input signal of 100 kHz.